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1 The architecture of replica: A special-purpose computer system for active multi-sensory perception of 3-dimentional objects

Y. W. Ma, R. Krishnamurti

January 1984 **ACM SIGARCH Computer Architecture News , Proceedings of the 11th annual international symposium on Computer architecture**, Volume 12 Issue 3

Full text available: pdf(668.60 KB) Additional Information: full citation, abstract, references, citings, index terms

REPLICA is a special-purpose computer architecture to support active multi-sensory perception of 3-D objects. The system is partitionable, reconfigurable, and highly parallel. In this paper, we present the design of a set of interconnection networks which form the core of the REPLICA architecture. This set of interconnection networks consists of a capability-enhanced cross-bar switch and multiple fast shift-register rings. The capability-enhanced cross-bar switch supports rapid set-up of pa ...

2 An efficient and effective performance evaluation method for multiprogrammed multiprocessor systems

Keqin LI

April 1997 **Proceedings of the 1997 ACM symposium on Applied computing**

Full text available: pdf(1.02 MB) Additional Information: full citation, references, index terms

Keywords: multi-server queueing system, partitionable parallel system, performance evaluation, response time, scheduling policy, shared memory multiprocessor system, utilization

3 Multiprocessor SoC: design strategies and programming models: Automatic synthesis of system on chip multiprocessor architectures for process networks

Basant Kumar Dwivedi, Anshul Kumar, M. Balakrishnan

September 2004 **Proceedings of the 2nd IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis**

Full text available: pdf(222.66 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we present an approach for automatic synthesis of System on Chip (SoC) multiprocessor architectures for applications expressed as process networks. Our approach is targeted towards design space exploration (DSE) and thus the speed of synthesis is of critical interest. The focus here is on the problem of resource allocation and binding with a view to optimize cost under performance constraints. Our approach exploits adjacency relation of processes and uses a dynamic programming bas ...

Terms used **multiprocessor cache crossbar** Found **334** of **148,786**

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1 C²MP: a cache-coherent, distributed memory multiprocessor-system
D. E. Marquardt, H. S. Alkhatib
August 1989 **Proceedings of the 1989 ACM/IEEE conference on Supercomputing**
Full text available: pdf(1.22 MB) Additional Information: full citation, abstract, references, citings, index terms

Current research into the problems of cache coherency in multiprocessor (MP) systems, has primarily focused on bus based memory interconnection networks (M-ICN) and the use of various types of "snooping" cache coherency protocols. Bus bandwidth limitations can be alleviated through the use of wider bandwidth general interconnection structures, such as a crossbar switch. However, if private caches are used, the cache coherency problem becomes mul ...

2 Multiprocessors with a serial multiport memory and a pseudo crossbar of serial links used s a processor-memeory switch
Daniel Litaize, Omar Hammami, Mustapha Lalam, Adelaziz Mzoughi, Pascl Sinrat
December 1989 **ACM SIGARCH Computer Architecture News**, Volume 17 Issue 6
Full text available: pdf(1.07 MB) Additional Information: full citation, abstract, citings, index terms

This paper presents an inventive information exchange pro-cess between the main memory and cache equipped processors. It makes use of serial multiport memories and high throughput serial transmission supports. It is then possible to consider the realization of a multiprocessor with a common memory shared by several hundreds processors set with a performance level close to that of a crossbar network one's without having its disadvantages. This exchange process generates a family of possible archi ...

3 Evaluation of design alternatives for a multiprocessor microprocessor
Basem A. Nayfeh, Lance Hammond, Kunle Olukotun
May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd annual international symposium on Computer architecture**, Volume 24 Issue 2
Full text available: pdf(1.37 MB) Additional Information: full citation, abstract, references, citings, index terms

In the future, advanced integrated circuit processing and packaging technology will allow for several design options for multiprocessor microprocessors. In this paper we consider three architectures: shared-primary cache, shared-secondary cache, and shared-memory. We evaluate these three architectures using a complete system simulation environment which models the CPU, memory hierarchy and I/O devices in sufficient detail to boot and run a commercial operating system. Within our simulation envir ...

4 Exploring the design space for a shared-cache multiprocessor
B. A. Nayfeh, K. Olukotun